09/682 233

TRANSMITTAL LETTER (General - Patent Issued)	Docket No. BUR920010042US1

Patentee(s): **Bernstein, *et al.***

U.S. Patent No.	Issue Date
7,000,162	**February 14, 2006**

Title: **INTEGRATED CIRCUIT PHASE PARTITIONED POWER DISTRIBUTION FOR STRESS POWER REDUCTION**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Certificate of Correction (2 pages) **(USPTO Error)**
Postcard

☒ No additional fee is required.
☐ A check in the amount of is attached.
☒ The Director is hereby authorized to charge and credit Deposit Account **09-0456 (IBM)** as described below.
  ☐ Charge the amount of
  ☒ Credit any overpayment.
  ☒ Charge any additional fee required.
☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Jack P. Friedman
Signature

Dated: **03/03/2006**

Jack P. Friedman
Reg. No. 44,688
Schmeiser, Olsen & Watts
3 Lear Jet Lane, Suite 201
Latham, New York 12110
(518) 220-1850

Customer No.: **30449**

cc:

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on **March 3, 2006**.
(Date)

Tina Holford
Signature of Person Mailing Correspondence

Tina Holford
Typed or Printed Name of Person Mailing Correspondence

DOC Code: COCIN

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : **7,000,162**

APPLICATION NO. : **09,682,233**

ISSUE DATE : **02/14/2006**

INVENTOR(S) : **Bernstein, *et al.***

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please add the entire "Summary of the Invention" as indicated on page 2 of 2. It was omitted in the Letters Patent.

Column 7
Line 30, delete "whore" and insert -- where --

Column 8
Line 44, delete "arc" and insert -- are --

Column 9
Line 54, delete "tail" and insert -- rail --

Column 10
Line 36, delete "front" and insert -- from --

Column 11
Line 56, delete "or" and insert -- of --

MAILING ADDRESS OF SENDER (Please do not use customer number

Jack P. Friedman, Ph.D. Reg. No.: 44,688
Schmeiser, Olsen & Watts
3 Lear Jet Lane, Suite 201
Latham, New York 12110

DOC Code: COCIN

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : **7,000,162**

APPLICATION NO. : **09/682,233**

ISSUE DATE : **02/14/2006**

INVENTOR(S) : **Bernstein *et al.***

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

SUMMARY OF THE INVENTION

A first aspect of the present invention is an integrated circuit device, comprising: a first power rail for supplying power to a first latch and a circuit during a first clock phase; a second power rail for supplying power to a second latch during a second clock phase; and the circuit coupled between an output of the first latch and an input of the second latch.

A second aspect of the present invention is an integrated circuit device, comprising: a first power rail for supplying power to an L1 latch of an L1/L2 latch during a first clock phase; and a second power rail for supplying power to an L2 latch of the L1/L2 latch and to a circuit coupled to an output of the L2 latch during a second clock phase.

A third aspect of the present invention is an integrated circuit device, comprising: a first power rail for supply power to first latch and a first circuit during a first clock phase; a second power rail for supplying power to a second latch and a second circuit during a second clock phase; a third power rail for supplying power to a third latch and a third circuit during a third clock phase; a fourth power rail for supply power to fourth latch and a fourth circuit during a fourth clock phase; and the first circuit coupled between an output of the first latch and an input of the second latch, the second circuit coupled between an output of the second latch and an input of the third latch, the third circuit coupled between an output of the third latch and an input of the fourth latch and the fourth circuit coupled to an output of the fourth latch.

A fourth aspect of the present invention is a method of stressing an integrated circuit device, the integrated circuit device including a first power rail for supplying power to first latch and a circuit, a second power rail for supplying power to a second latch, and the circuit coupled between an output of the first latch and an input of the second latch, comprising: powering the power rail during each phase of a first clock; and powering the second power rail each phase of a second clock.

A fifth aspect of the present invention is a method of stressing an integrated circuit device, the integrated circuit device including a first power rail for supplying power to an L1 latch of an L1/L2 latch; and a second power rail for supplying power to an L2 latch of the L1/L2 latch and to a circuit coupled to an output of the L2 latch, comprising:powering the first power rail during each phase of a first clock; and powering the second power rail during each phase of a second clock.

A sixth aspect of the present invention is a method of stressing an integrated circuit device, the integrated circuit device including a first power rail for supply power to first latch and a first circuit, a second power rail for supplying power to a second latch and a second circuit, a third power rail for supplying power to a third latch and a third circuit, a fourth power rail for supply power to fourth latch and a fourth circuit, and the first circuit coupled between an output of the first latch and an input of the second latch, the second circuit coupled between an output of the second latch and an input of the third latch, the third circuit coupled between an output of the third latch and an input of the fourth latch and the fourth circuit coupled to an output of the fourth latch, comprising: powering the first power rail during each phase of a first clock; powering the second power rail during each phase of a second clock; powering the third power rail during each phase of a third clock; and powering the fourth power rail during each phase of a fourth clock.

MAILING ADDRESS OF SENDER (Please do not use customer number

Jack P. Friedman, Ph.D. Reg. No.: 44,688
Schmeiser, Olsen & Watts
3 Lear Jet Lane, Suite 201
Latham, New York 12110

MAR 10 2006